CLOCKING SCHEME FOR AN ALGORITHMIC ANALOG-TO-DIGITAL CONVERTER

Abstract

[91] An algorithmic analog-to-digital converter (ADC) includes a sample-and-hold circuit and an ADC processing unit operating in parallel and sharing a single operational amplifier. The ADC processing unit includes an MDAC with a switched capacitor topology and a sub-ADC. The ADC processing unit is clocked by an internal clock that is N times faster than the sample-and-hold clock. Each cycle is further sub-divided into two phases. During one phase the capacitors are coupled to a residue or sampled voltage provided by the MDAC, and during another phase the capacitor are coupled to a reference voltage determined by the switch control signals generated by the sub-ADC. A set of data bits is generated by the ADC processing unit during each ADC clock cycle. The N sets of data bits are added to generate the digital output stream. The internal clock, in turn, has a variable period allocating more time to the early operation phases where more accuracy is required and less time to the latter operation phases where less accuracy is required.